NCP1450A

PWM Step-up DC-DC Controller

The NCP1450A series are PWM step−up DC−DC switching controller that are specially designed for powering portable equipment from one or two cells battery packs. The NCP1450A series have a driver pin, EXT pin, for connecting to an external transistor. Large output currents can be obtained by connecting a low ON−resistance external power transistor to the EXT pin. The device will automatically skip switching cycles under light load condition to maintain high efficiency at light loads. With only six external components, this series allows a simple means to implement highly efficient converter for large output current applications.

Each device consists of an on−chip Pulse Width Modulation (PWM) oscillator, PWM controller, phase−compensated error amplifier, soft−start, voltage reference, and driver for driving external power transistor. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1450A device series are available in the TSOP−5 package with five standard regulated output voltages. Additional voltages that range from 1.8 V to 5.0 V in 100 mV steps can be manufactured.

Features

- High Efficiency 86% at I_O = 200 mA, V_{IN} = 2.0 V, V_{OUT} = 3.0 V
  88% at I_O = 400 mA, V_{IN} = 3.0 V, V_{OUT} = 5.0 V
- Low Startup Voltage of 0.9 V typical at I_O = 1.0 mA
- Operation Down to 0.6 V
- Five Standard Voltages: 1.9 V, 2.7 V, 3.0 V, 3.3 V, 5.0 V with High Accuracy ± 2.5%
- Low Conversion Ripple
- High Output Current up to 1000 mA
  (3.0 V version at V_{IN} = 2.0 V, L = 10 μH, C_{OUT} = 220 μF)
- Fixed Frequency Pulse Width Modulation (PWM) at 180 kHz
- Chip Enable Pin with On−chip 150 nA Pullup Current Source
- Low Profile and Micro Miniature TSOP−5 Package
- Pb−Free Packages are Available

Typical Applications

- Personal Digital Assistant (PDA)
- Electronic Games
- Portable Audio (MP3)
- Digital Still Cameras
- Handheld Instruments

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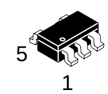
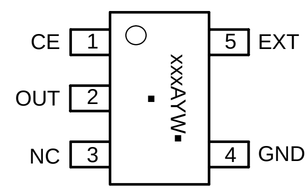


TSOP−5
SN SUFFIX
CASE 483

MARKING DIAGRAM AND PIN CONNECTIONS



(Top View)

xxx =Specific Device Marking
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 3 of this data sheet.

December, 2005 − Rev. 7

Publication Order Number:
NCP1450A/D

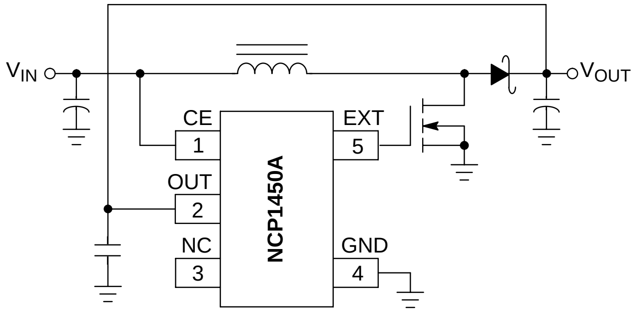


Figure 1. Typical Step−up Converter Application

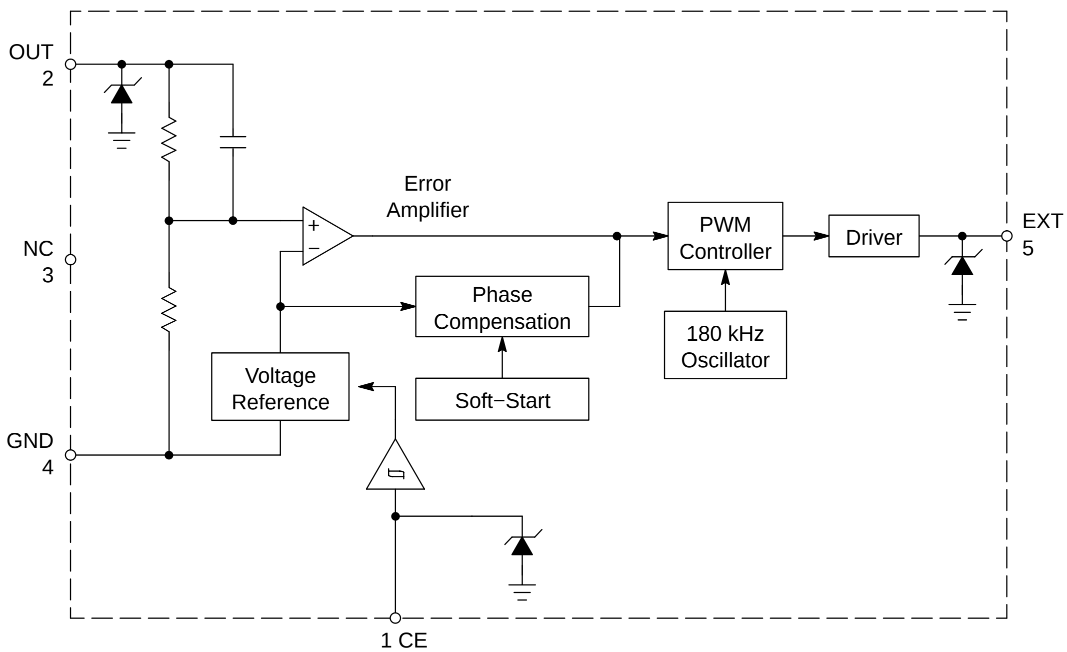


Figure 2. Representative Block Diagram

PIN FUNCTION DESCRIPTION

Pin #	Symbol	Pin Description
1	CE	Chip Enable Pin (1) The chip is enabled if a voltage equal to or greater than 0.9 V is applied. (2) The chip is disabled if a voltage less than 0.3 V is applied. (3) The chip is enabled if this pin is left floating.
2	OUT	Output voltage monitor pin and also the power supply pin for the device.
3	NC	No internal connection to this pin.
4	GND	Ground pin.
5	EXT	External transistor drive pin.

ORDERING INFORMATION (Note 1)

Device	Output Voltage	Switching Frequency	Marking	Package	Shipping†
NCP1450ASN19T1	1.9 V	180 KHz	DAY	TSOP−5	3000 Units on 7 Inch Reel
NCP1450ASN19T1G				TSOP−5 (Pb−Free)	
NCP1450ASN27T1G	2.7 V		DAZ	TSOP−5	
NCP1450ASN27T1				TSOP−5 (Pb−Free)	
NCP1450ASN30T1	3.0 V		DBA	TSOP−5	
NCP1450ASN30T1G				TSOP−5 (Pb−Free)	
NCP1450ASN33T1	3.3 V		DBC	TSOP−5	
NCP1450ASN33T1G				TSOP−5 (Pb−Free)	
NCP1450ASN50T1	5.0 V		DBD	TSOP−5	
NCP1450ASN50T1G				TSOP−5 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. The ordering information lists five standard output voltage device options. Additional devices with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 2)	V_{OUT}	6.0	V
Input/Output Pins EXT (Pin 5) EXT Sink/Source Current	 V_{EXT} I_{EXT}	 −0.3 to 6.0 −150 to 150	 V mA
CE (Pin 1) Input Voltage Range Input Current Range	 V_{CE} I_{CE}	 −0.3 to 6.0 −150 to 150	 V mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction−to−Air	 P_D $R_{\theta JA}$	 500 250	 mW °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
3. Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (For all values T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{OUT} = V_{SET} × 0.96, Note 5)	f_{OSC}	144	180	216	kHz
Frequency Temperature Coefficient (T_A = −40°C to 85°C)	Δf	−	0.11	−	%/°C
Maximum PWM Duty Cycle (V_{OUT} = V_{SET} × 0.96)	D_{MAX}	70	80	90	%
Minimum Startup Voltage (I_O = 0 mA)	V_{start}	−	0.8	0.9	V
Minimum Startup Voltage Temperature Coefficient (T_A = −40°C to 85°C)	ΔV_{start}	−	−1.6	−	mV/°C
Minimum Operation Hold Voltage (I_O = 0 mA)	V_{hold}	−	0.6	0.7	V
Soft−Start Time (V_{OUT} = V_{SET}, Note 6)	t_{SS}	−	100	250	ms
CE (PIN 1)					
CE Input Voltage (V_{OUT} = V_{SET} × 0.96)					V
High State, Device Enabled	$V_{CE(high)}$	0.9	−	−	
Low State, Device Disabled	$V_{CE(low)}$	−	−	0.3	
CE Input Current (Note 6)					μA
High State, Device Enabled (V_{OUT} = V_{CE} = 5.0 V)	$I_{CE(high)}$	−0.5	0	0.5	
Low State, Device Disabled (V_{OUT} = 5.0 V, V_{CE} = 0 V)	$I_{CE(low)}$	0	0.15	0.5	
EXT (PIN 5)					
EXT “H” Output Current (V_{EXT} = V_{OUT} −0.4 V)	I_{EXTH}				mA
Device Suffix:					
19T1		−	−25.0	−20.0	
27T1		−	−35.0	−30.0	
30T1		−	−37.7	−30.0	
33T1		−	−40.0	−30.0	
50T1		−	−53.7	−35.0	
EXT “L” Output Current(V_{EXT} = 0.4 V)	I_{EXTL}				mA
Device Suffix:					
19T1		20.0	38.3	−	
27T1		30.0	48.0	−	
30T1		30.0	50.8	−	
33T1		30.0	52.0	−	
50T1		35.0	58.2	−	
TOTAL DEVICE					
Output Voltage	V_{OUT}				V
Device Suffix:					
19T1		1.853	1.9	1.948	
27T1		2.633	2.7	2.768	
30T1		2.925	3.0	3.075	
33T1		3.218	3.3	3.383	
50T1		4.875	5.0	5.125	
Output Voltage Temperature Coefficient (T_A = −40 to +85°C)	ΔV_{OUT}	−	150	−	ppm/°C
Operating Current (V_{OUT} = V_{CE} = V_{SET} × 0.96, Note 5)	I_{DD}				μA
Device Suffix:					
19T1		−	55	90	
27T1		−	93	140	
30T1		−	98	150	
33T1		−	103	160	
50T1		−	136	220	
Standby Current (V_{OUT} = V_{CE} = V_{SET} +0.5 V)	I_{STB}	−	15	20	μA
Off−State Current (V_{OUT} = 5.0 V, V_{CE} = 0 V, T_A = −40 to +85°C, Note 7)	I_{OFF}	−	0.6	1.5	μA

5. V_{SET} means setting of output voltage.
6. This parameter is guaranteed by design.
7. CE pin is integrated with an internal 150 nA pullup current source.

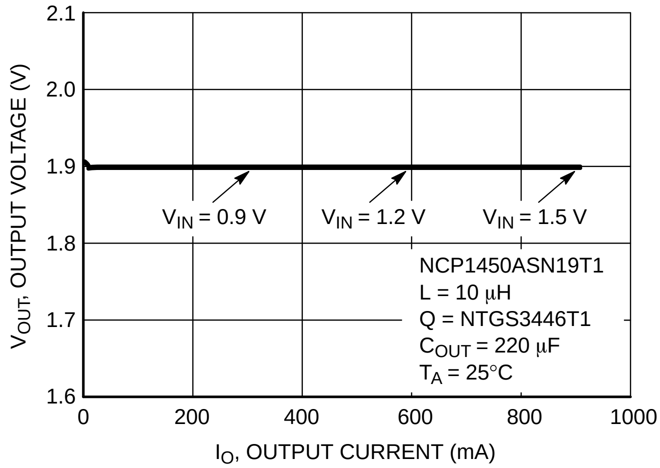


Figure 3. NCP1450ASN19T1 Output Voltage vs. Output Current

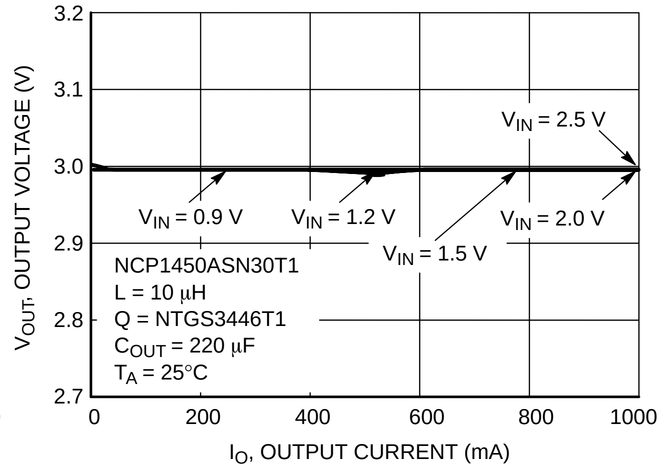


Figure 4. NCP1450ASN30T1 Output Voltage vs. Output Current

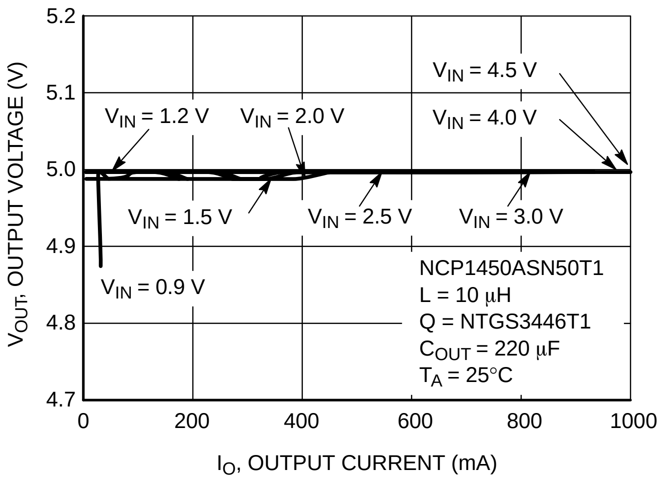


Figure 5. NCP1450ASN50T1 Output Voltage vs. Output Current

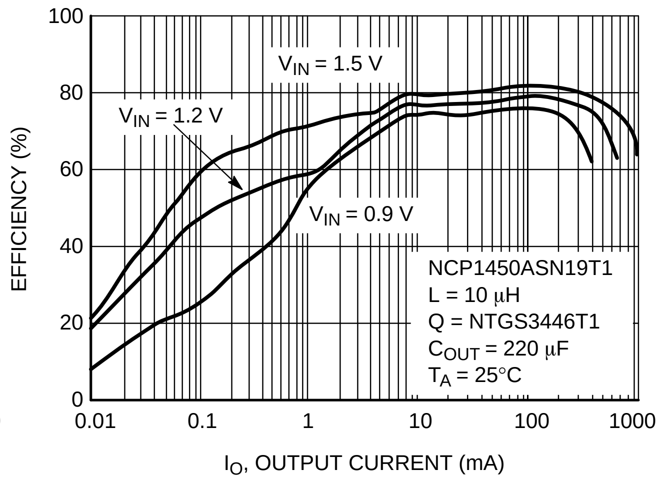


Figure 6. NCP1450ASN19T1 Efficiency vs. Output Current

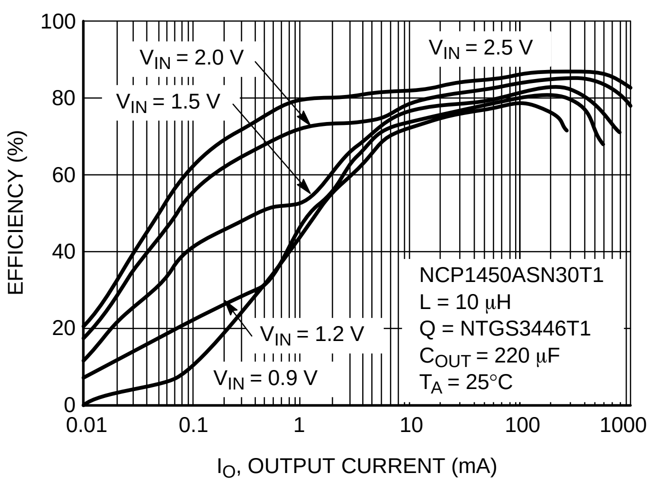


Figure 7. NCP1450ASN30T1 Efficiency vs. Output Current

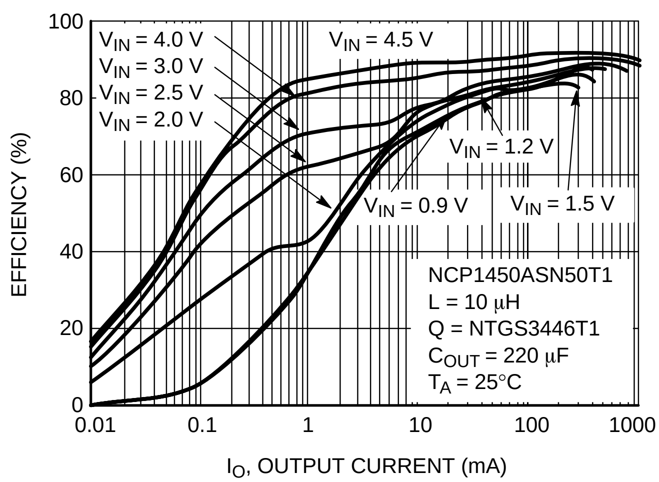


Figure 8. NCP1450ASN50T1 Efficiency vs. Output Current

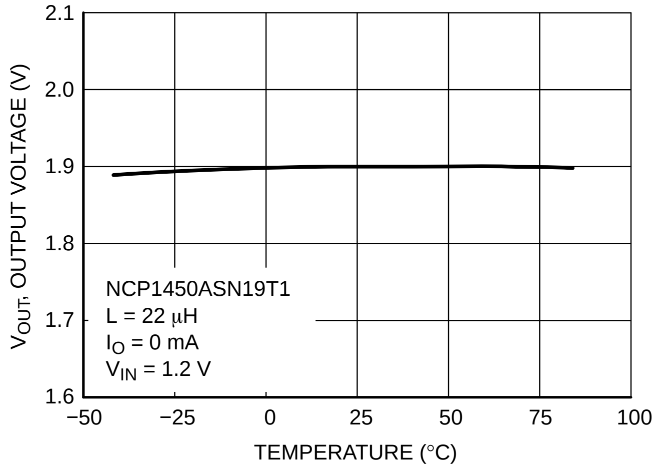


Figure 9. NCP1450ASN19T1 Output Voltage vs. Temperature

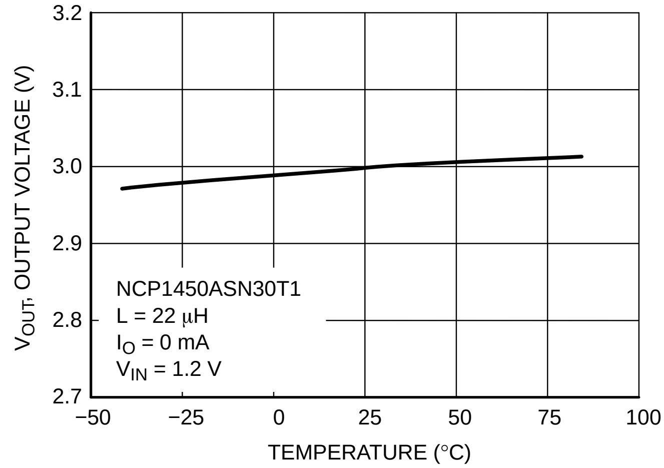


Figure 10. NCP1450ASN30T1 Output Voltage vs. Temperature

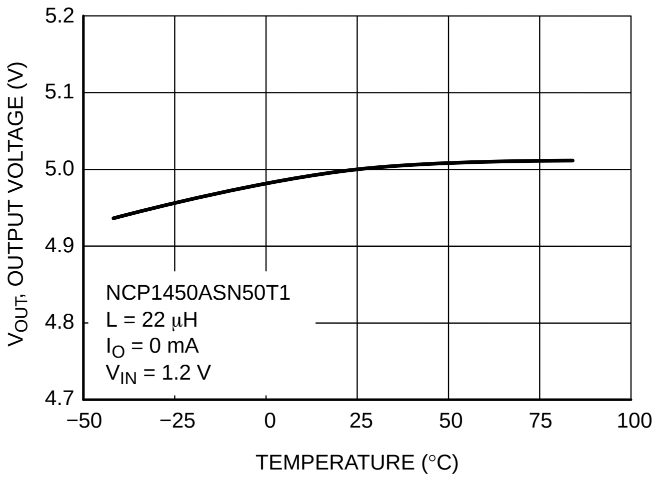


Figure 11. NCP1450ASN50T1 Output Voltage vs. Temperature

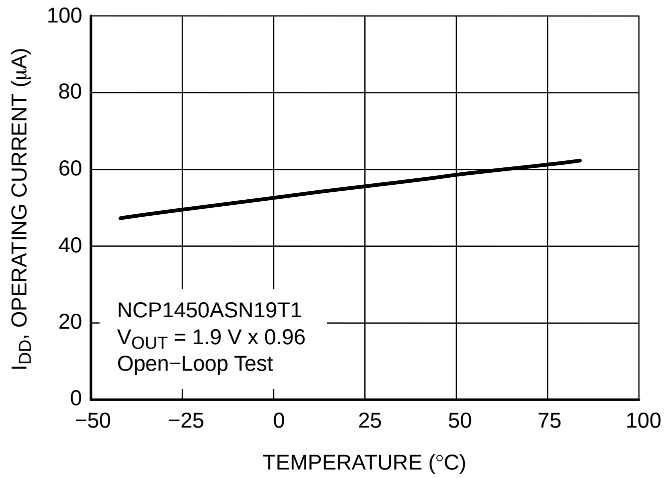


Figure 12. NCP1450ASN19T1 Operating Current vs. Temperature

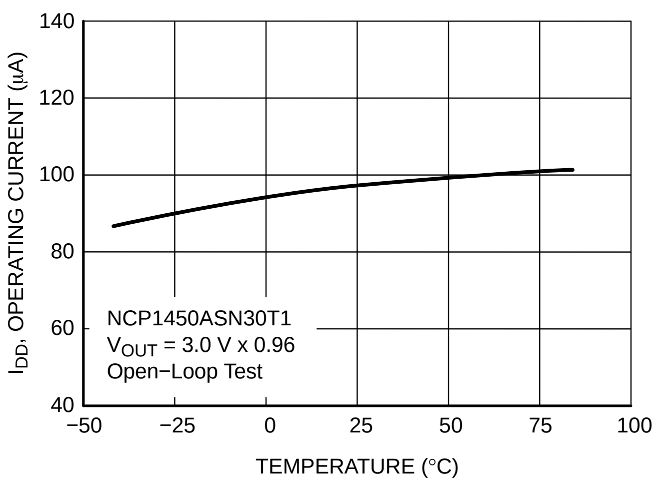


Figure 13. NCP1450ASN30T1 Operating Current vs. Temperature

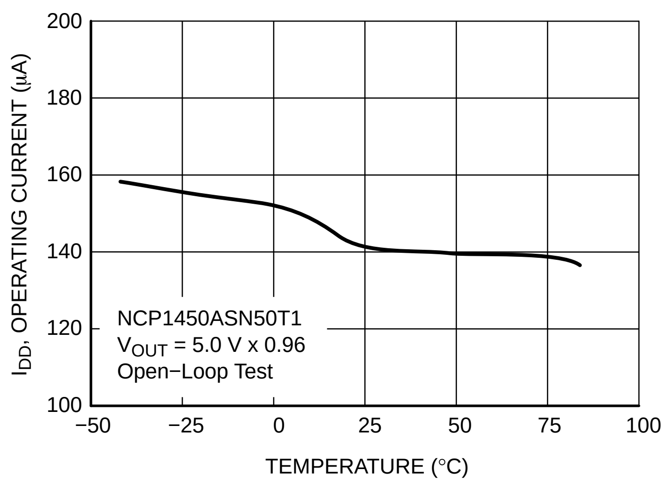


Figure 14. NCP1450ASN50T1 Operating Current vs. Temperature

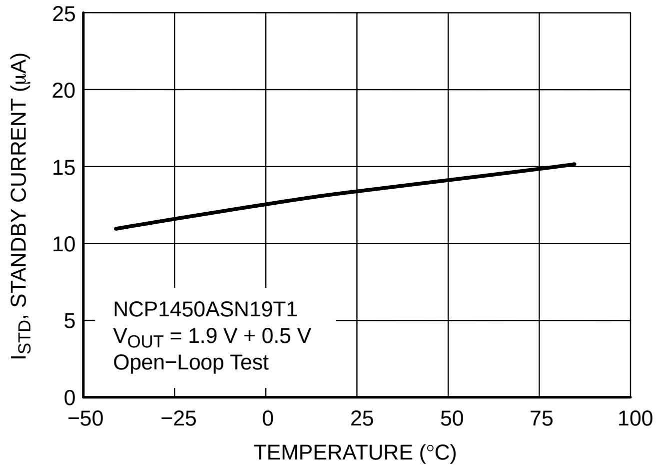


Figure 15. NCP1450ASN19T1 Standby Current vs. Temperature

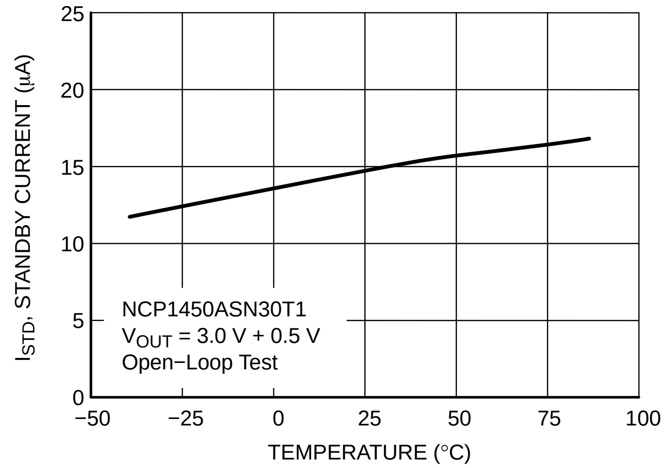


Figure 16. NCP1450ASN30T1 Standby Current vs. Temperature

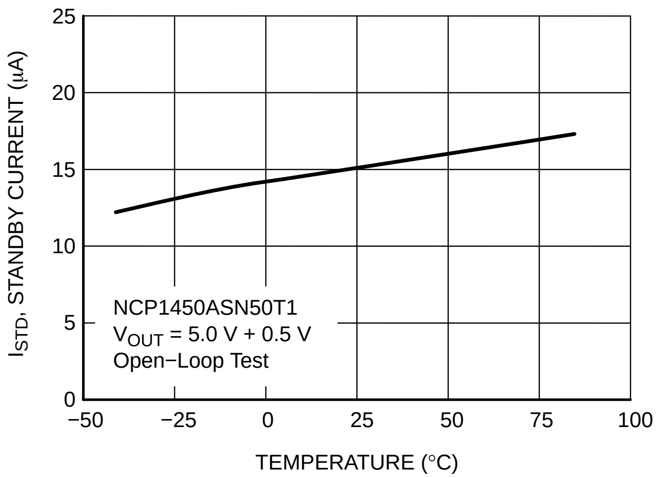


Figure 17. NCP1450ASN50T1 Standby Current vs. Temperature

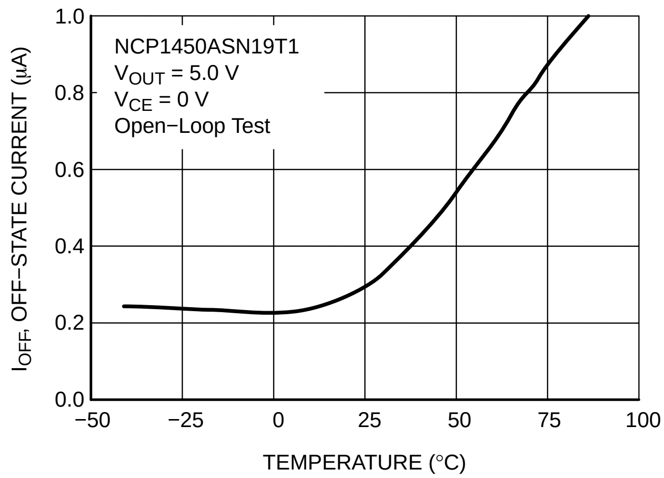


Figure 18. NCP1450ASN19T1 Off−State Current vs. Temperature

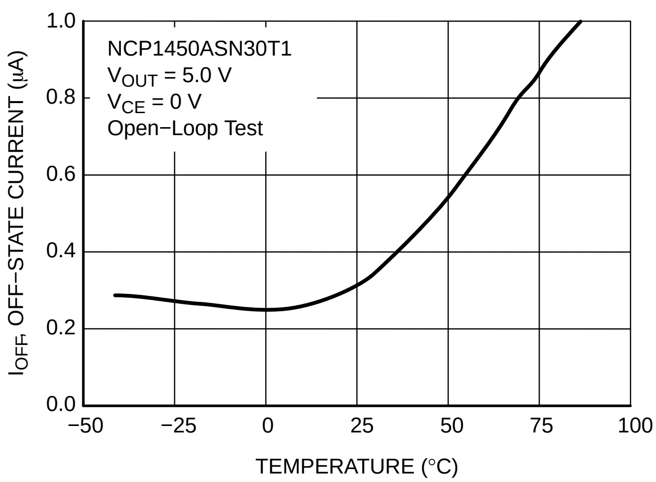


Figure 19. NCP1450ASN30T1 Off−State Current vs. Temperature

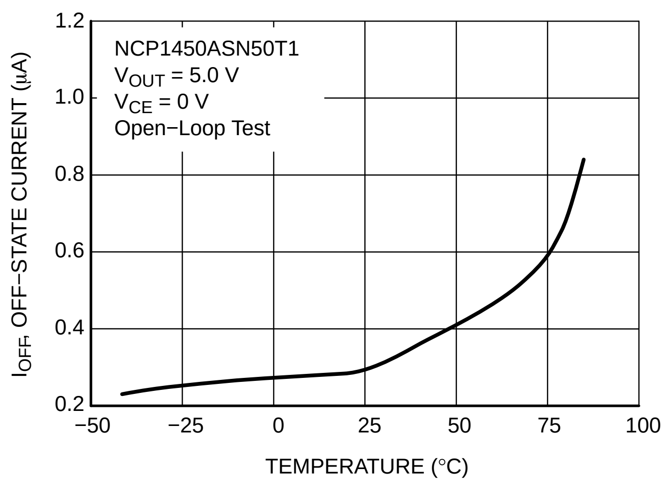


Figure 20. NCP1450ASN50T1 Off−State Current vs. Temperature

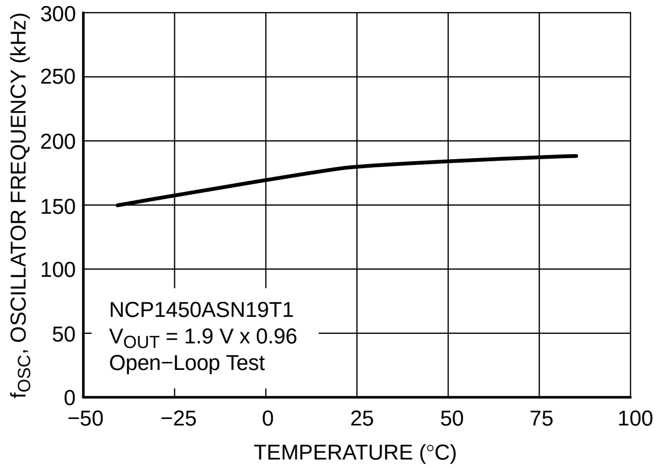


Figure 21. NCP1450ASN19T1 Oscillator Frequency vs. Temperature

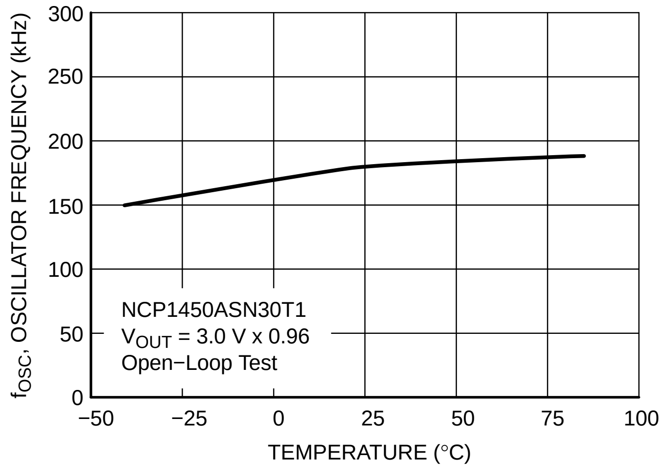


Figure 22. NCP1450ASN30T1 Oscillator Frequency vs. Temperature

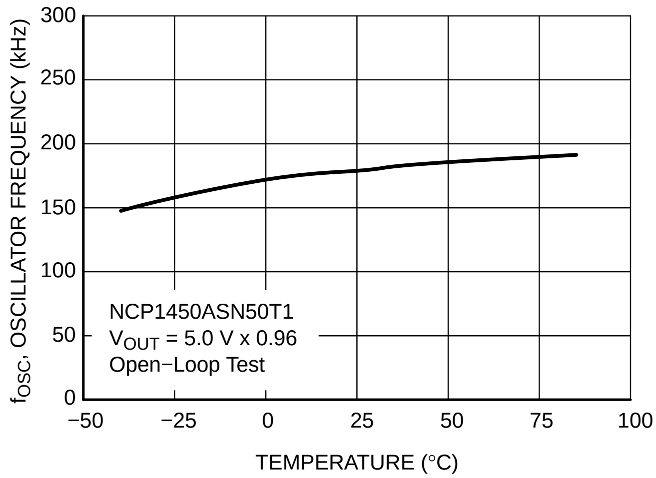


Figure 23. NCP1450ASN50T1 Oscillator Frequency vs. Temperature

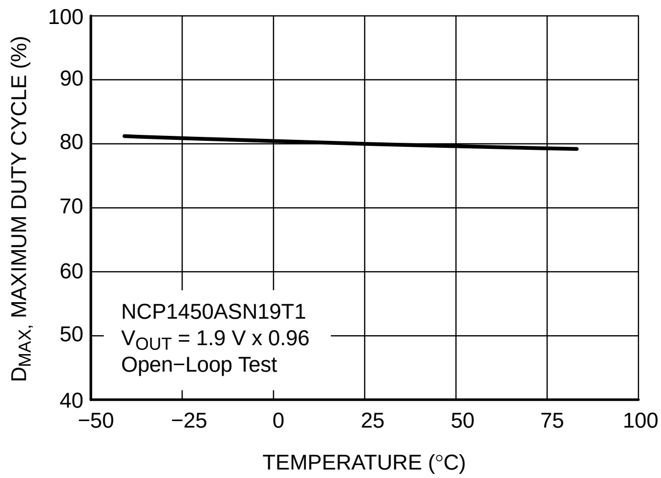


Figure 24. NCP1450ASN19T1 Maximum Duty Cycle vs. Temperature

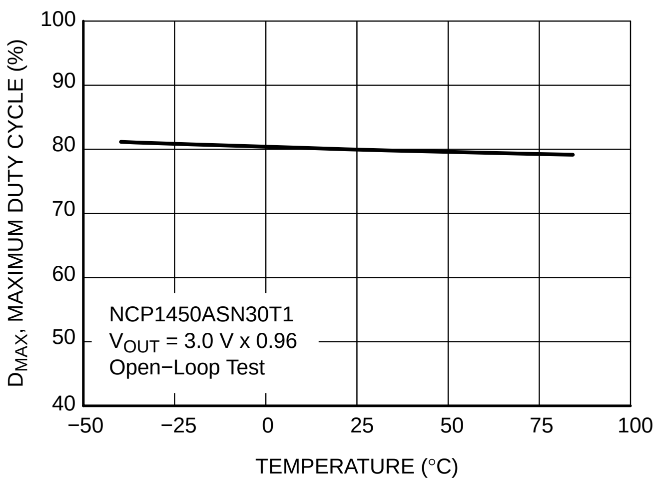


Figure 25. NCP1450ASN30T1 Maximum Duty Cycle vs. Temperature

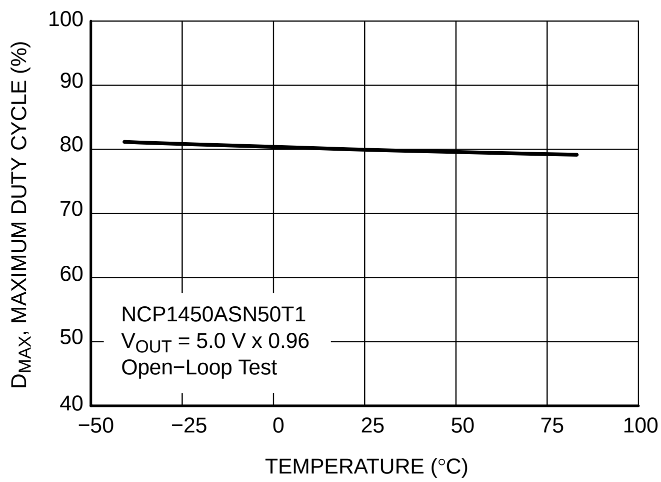


Figure 26. NCP1450ASN50T1 Maximum Duty Cycle vs. Temperature

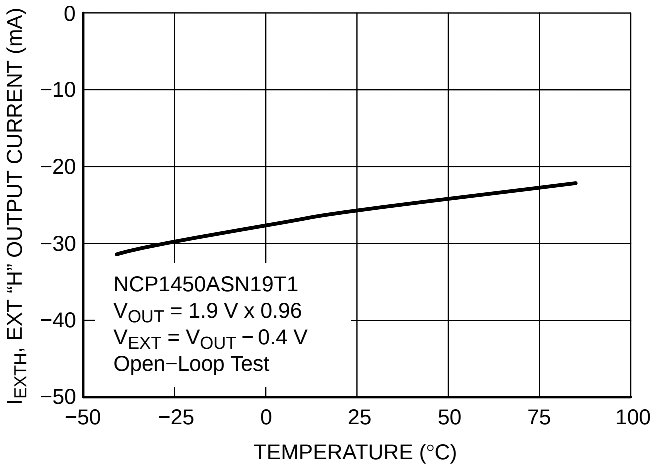


Figure 27. NCP1450ASN19T1 EXT “H” Output Current vs. Temperature

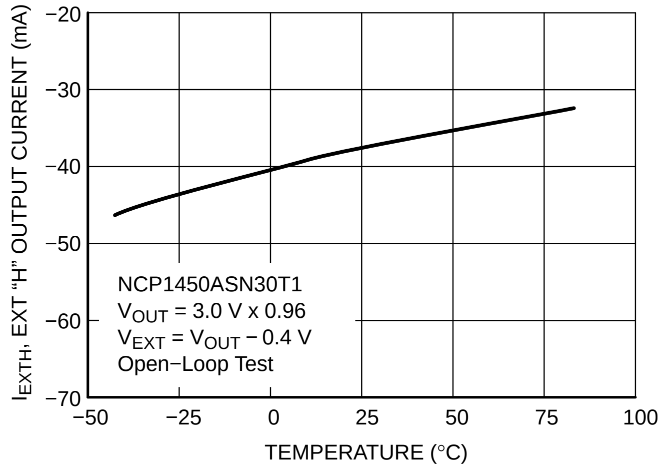


Figure 28. NCP1450ASN30T1 EXT “H” Output Current vs. Temperature

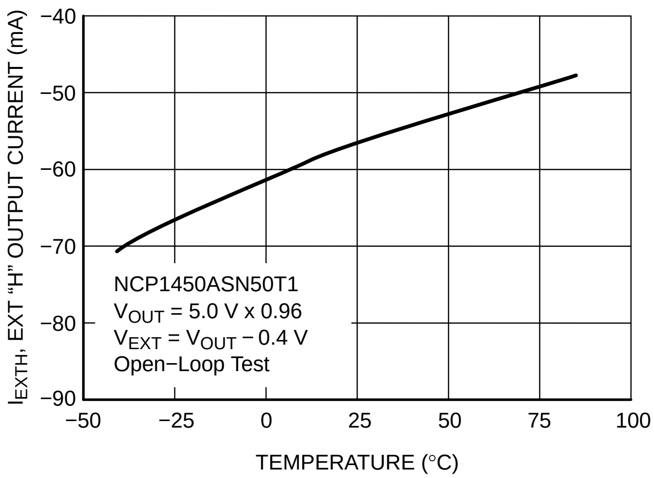


Figure 29. NCP1450ASN50T1 EXT “H” Output Current vs. Temperature

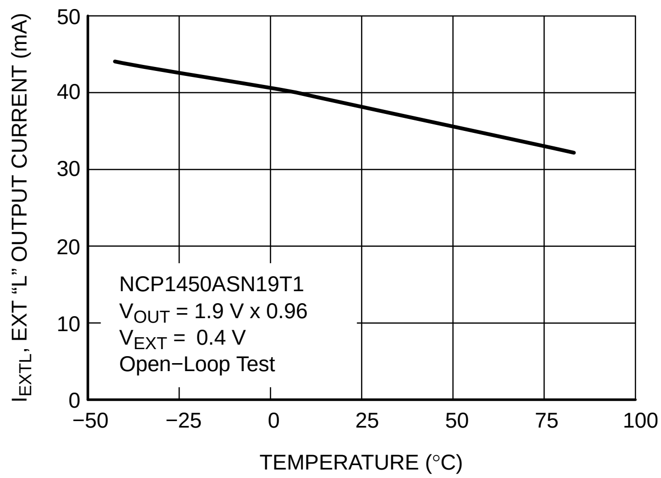


Figure 30. NCP1450ASN19T1 EXT “L” Output Current vs. Temperature

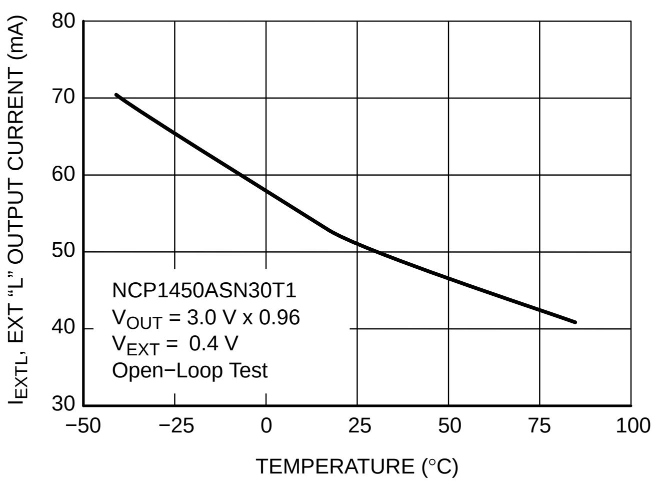


Figure 31. NCP1450ASN30T1 EXT “L” Output Current vs. Temperature

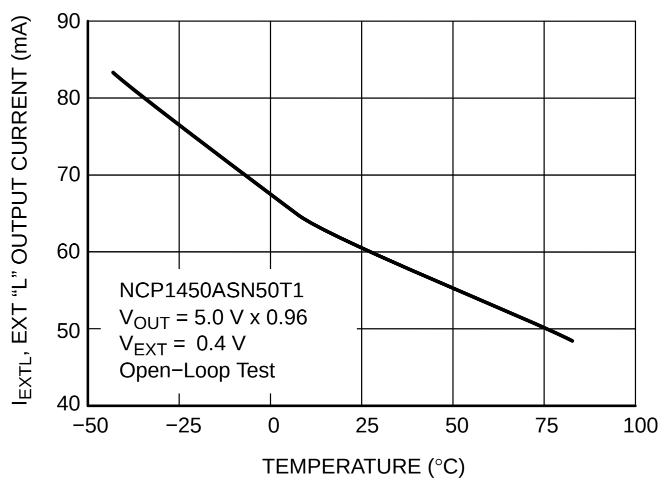


Figure 32. NCP1450ASN50T1 EXT “L” Output Current vs. Temperature

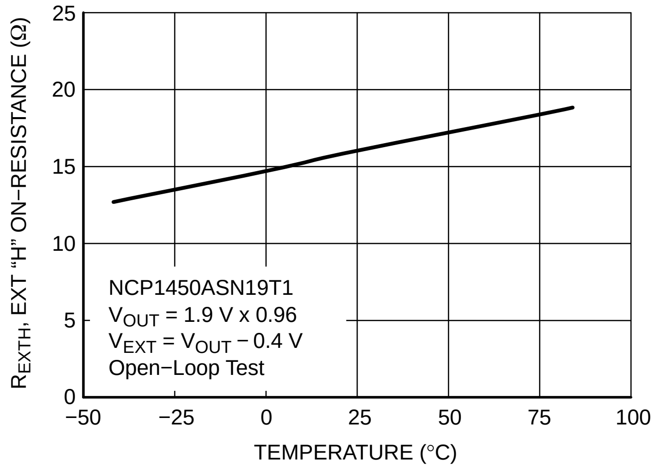


Figure 33. NCP1450ASN19T1 EXT "H" ON−Resistance vs. Temperature

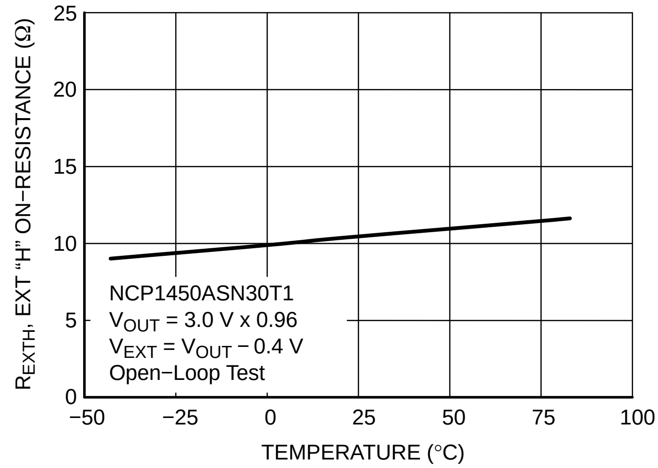


Figure 34. NCP1450ASN30T1 EXT "H" ON−Resistance vs. Temperature

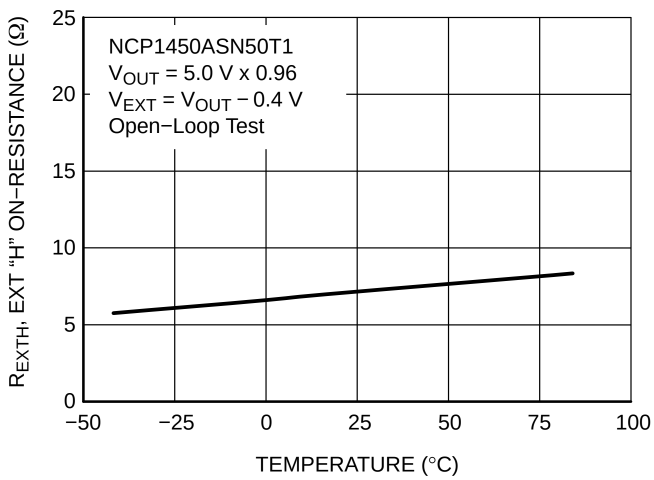


Figure 35. NCP1450ASN50T1 EXT "H" ON−Resistance vs. Temperature

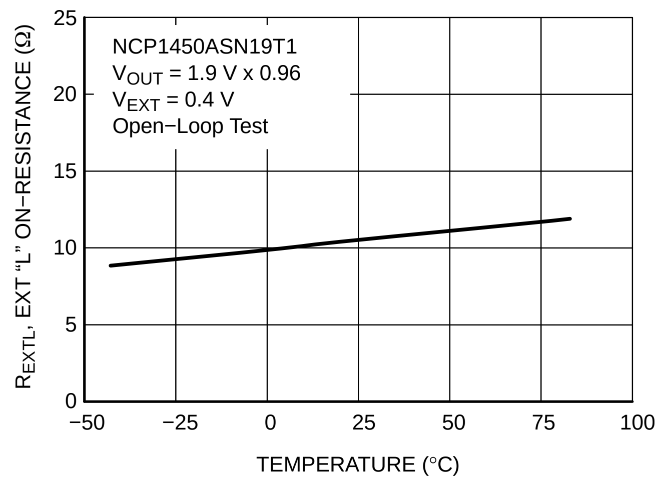


Figure 36. NCP1450ASN19T1 EXT "L" ON−Resistance vs. Temperature

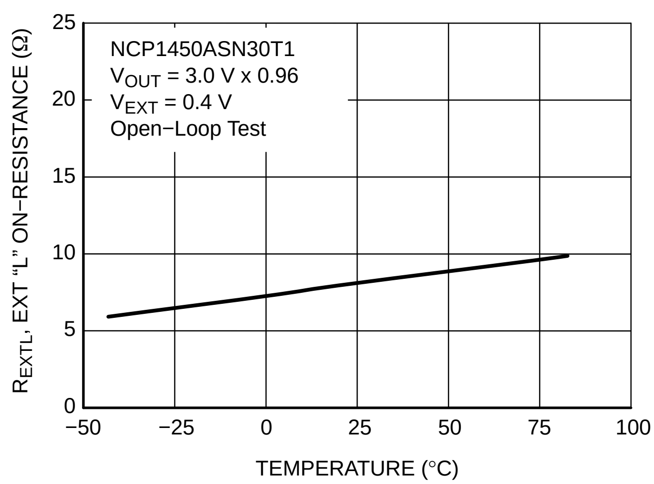


Figure 37. NCP1450ASN30T1 EXT "L" ON−Resistance vs. Temperature

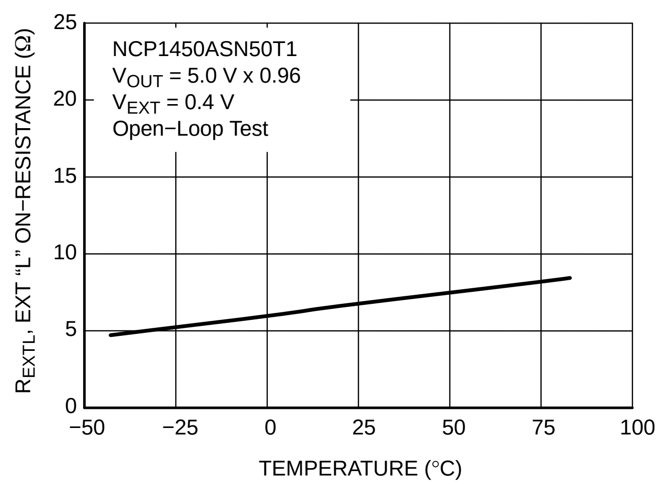


Figure 38. NCP1450ASN50T1 EXT "L" ON−Resistance vs. Temperature

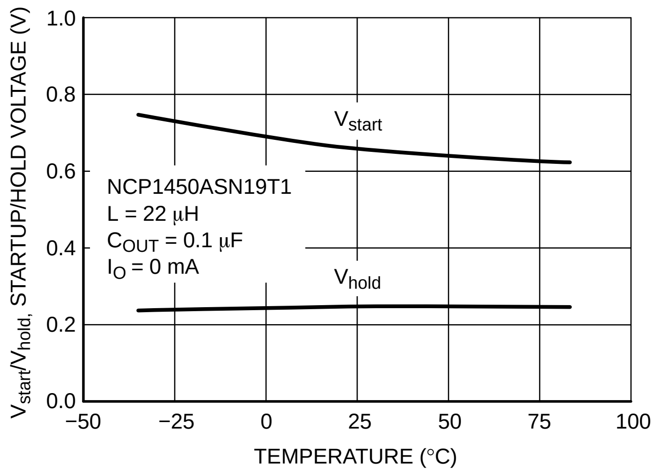


Figure 39. NCP1450ASN19T1 Startup/Hold Voltage vs. Temperature

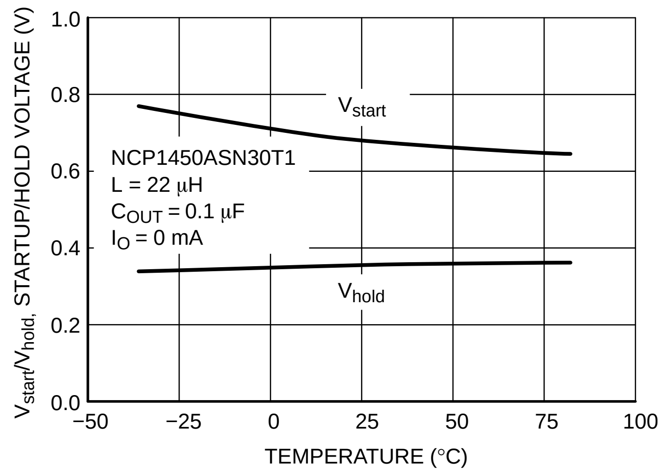


Figure 40. NCP1450ASN30T1 Startup/Hold Voltage vs. Temperature

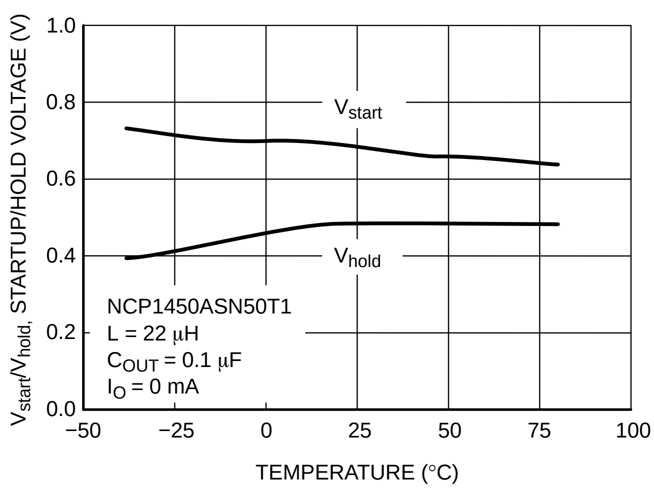


Figure 41. NCP1450ASN50T1 Startup/Hold Voltage vs. Temperature

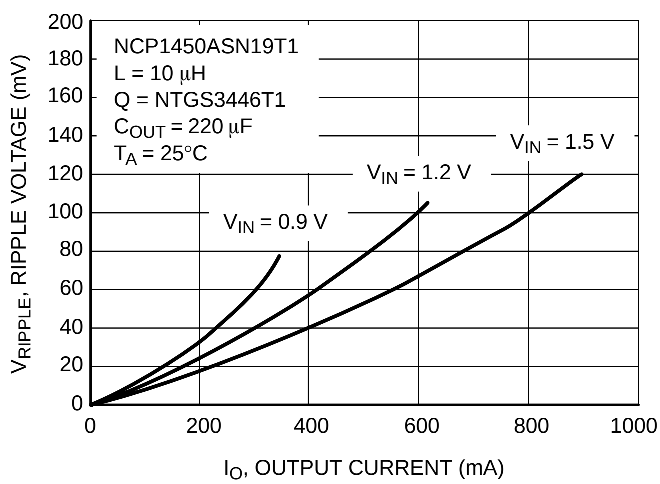


Figure 42. NCP1450ASN19T1 Ripple Voltage vs. Output Current

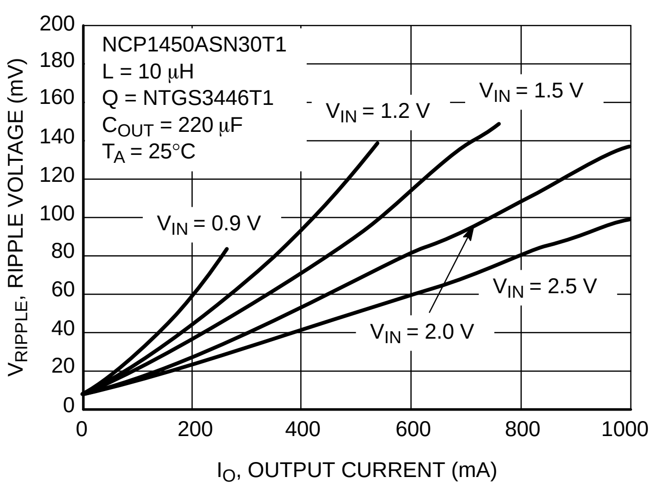


Figure 43. NCP1450ASN30T1 Ripple Voltage vs. Output Current

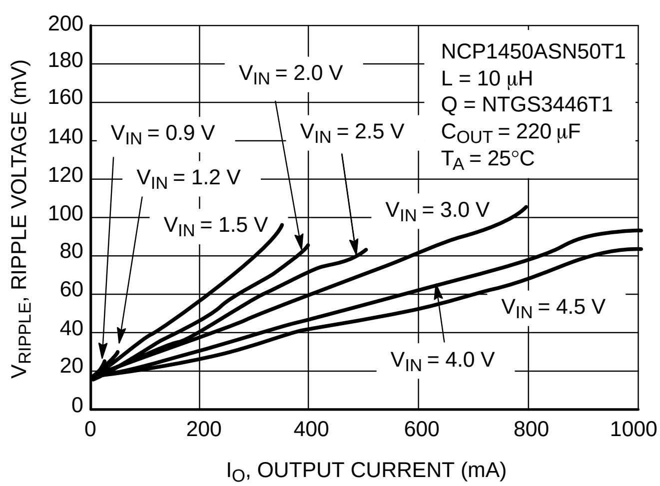


Figure 44. NCP1450ASN50T1 Ripple Voltage vs. Output Current

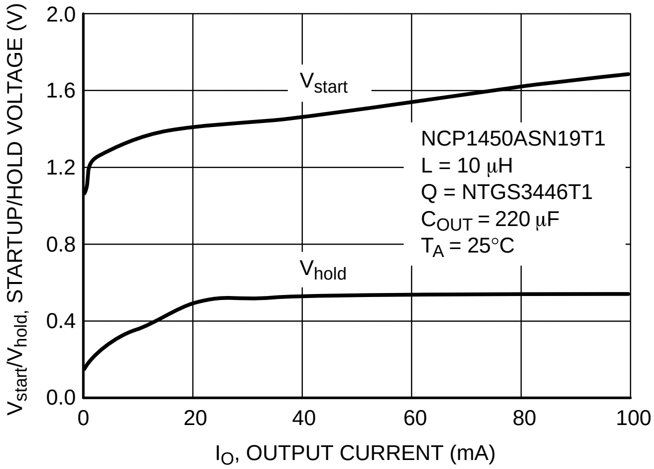


Figure 45. NCP1450ASN19T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)

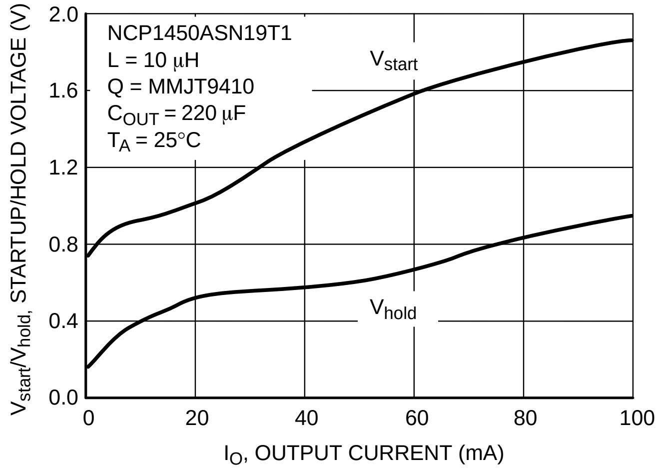


Figure 46. NCP1450ASN19T1 Startup/Hold Voltage vs. Output Current (Using BJT)

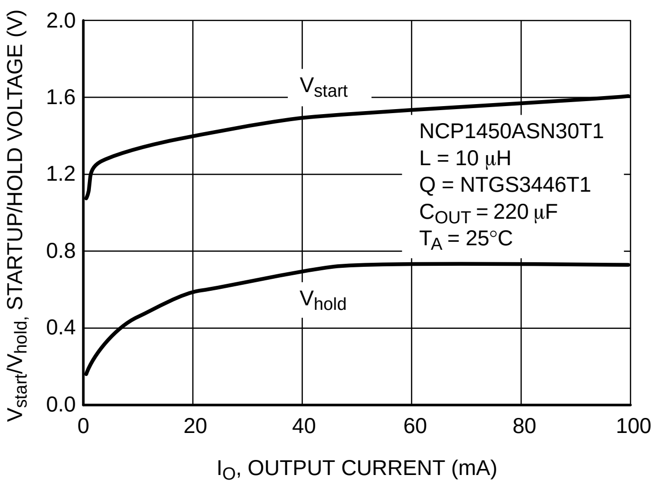


Figure 47. NCP1450ASN30T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)

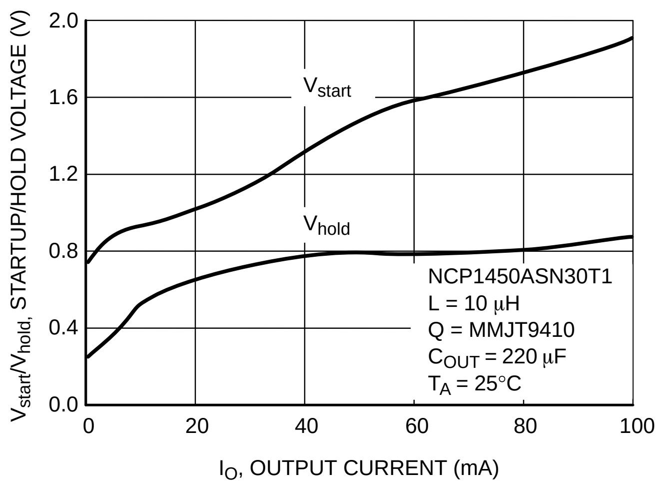


Figure 48. NCP1450ASN30T1 Startup/Hold Voltage vs. Output Current (Using BJT)

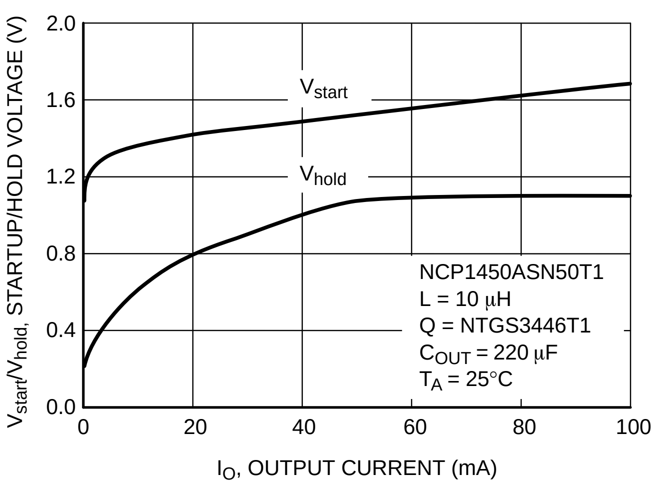


Figure 49. NCP1450ASN50T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)

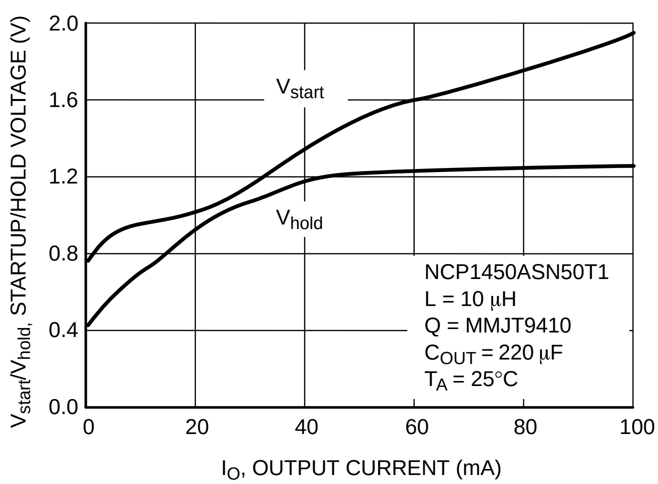
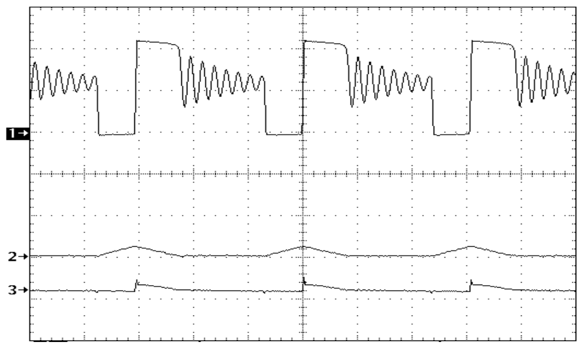
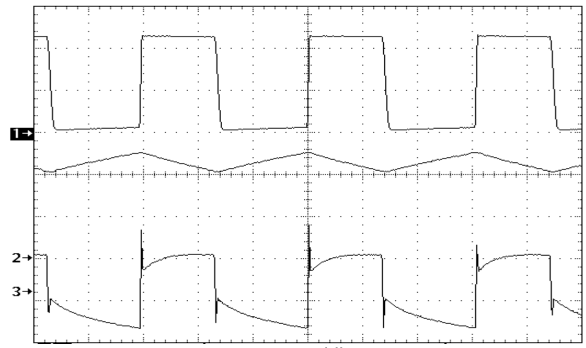


Figure 50. NCP1450ASN50T1 Startup/Hold Voltage vs. Output Current (Using BJT)



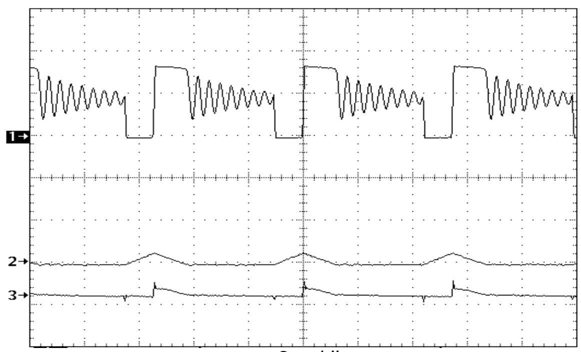
2 μs/div
V_{OUT} = 1.9 V, V_{IN} = 1.2 V, I_O = 20 mA, L = 10 μH,
C_{OUT} = 220 μF
1. V_L, 1.0 V/div
2. I_L, 500 mA/div
3. V_{OUT}, 50 mV/div, AC coupled

Figure 51. NCP1450ASN19T1 Operating Waveforms (Medium Load)



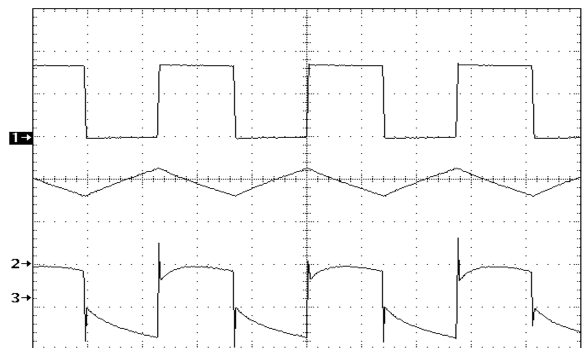
2 μs/div
V_{OUT} = 1.9 V, V_{IN} = 1.2 V, I_O = 500 mA, L = 10 μH,
C_{OUT} = 220 μF
1. V_L, 1.0 V/div
2. I_L, 500 mA/div
3. V_{OUT}, 50 mV/div, AC coupled

Figure 52. NCP1450ASN19T1 Operating Waveforms (Heavy Load)



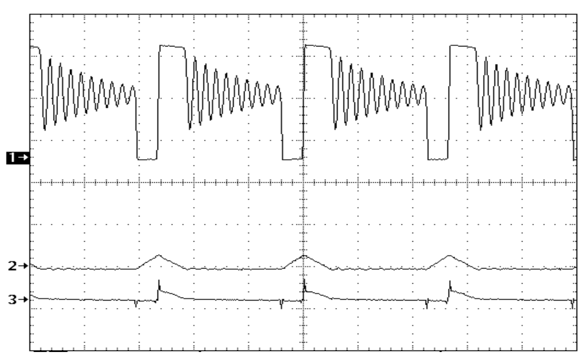
2 μs/div
V_{OUT} = 3.0 V, V_{IN} = 1.8 V, I_O = 20 mA, L = 10 μH,
C_{OUT} = 220 μF
1. V_L, 2.0 V/div
2. I_L, 500 mA/div
3. V_{OUT}, 50 mV/div, AC coupled

Figure 53. NCP1450ASN30T1 Operating Waveforms (Medium Load)



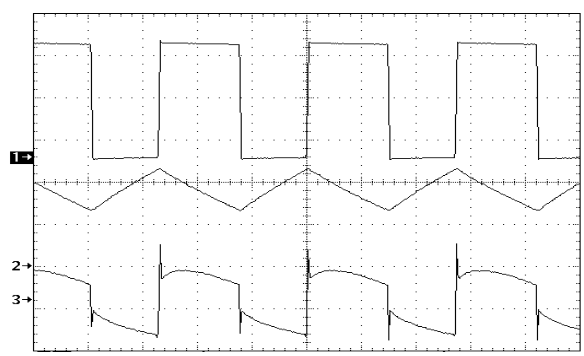
2 μs/div
V_{OUT} = 3.0 V, V_{IN} = 1.8 V, I_O = 500 mA, L = 10 μH,
C_{OUT} = 220 μF
1. V_L, 2.0 V/div
2. I_L, 500 mA/div
3. V_{OUT}, 50 mV/div, AC coupled

Figure 54. NCP1450ASN30T1 Operating Waveforms (Heavy Load)



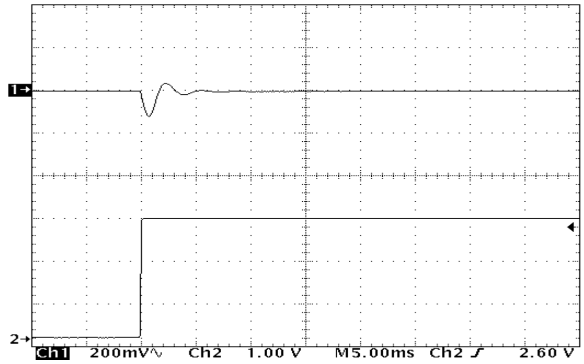
2 μs/div
V_{OUT} = 5.0 V, V_{IN} = 3.0 V, I_O = 20 mA, L = 10 μH,
C_{OUT} = 220 μF
1. V_L, 2.0 V/div
2. I_L, 500 mA/div
3. V_{OUT}, 50 mV/div, AC coupled

Figure 55. NCP1450ASN50T1 Operating Waveforms (Medium Load)



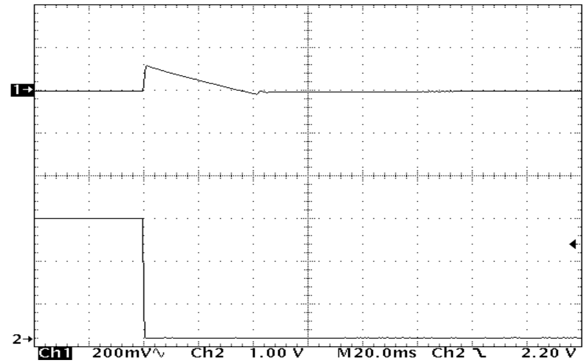
2 μs/div
V_{OUT} = 5.0 V, V_{IN} = 3.0 V, I_O = 500 mA, L = 10 μH,
C_{OUT} = 220 μF
1. V_L, 2.0 V/div
2. I_L, 500 mA/div
3. V_{OUT}, 50 mV/div, AC coupled

Figure 56. NCP1450ASN50T1 Operating Waveforms (Heavy Load)



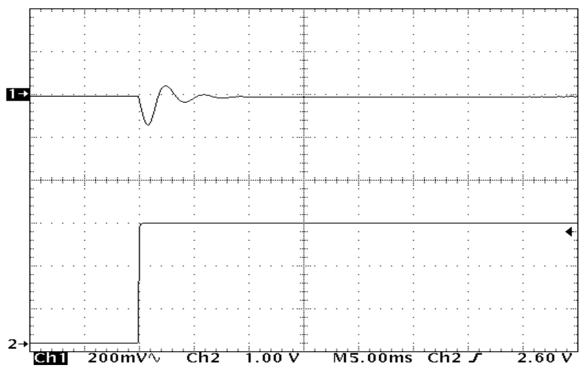
V_{IN} = 1.5 V, L = 4.7 μH, C_{OUT} = 220 μF
1. V_{OUT}, 1.9 V (AC coupled), 200 mV/div
2. I_O, 1.0 mA to 100 mA

Figure 57. NCP1450ASN19T1 Load Transient Response



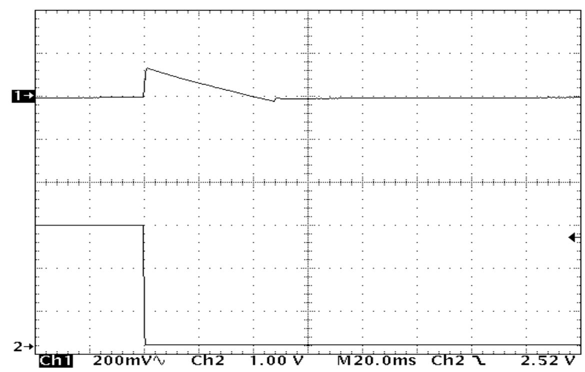
V_{IN} = 1.5 V, L = 4.7 μH, C_{OUT} = 220 μF
1. V_{OUT}, 1.9 V (AC coupled), 200 mV/div
2. I_O, 100 mA to 1.0 mA

Figure 58. NCP1450ASN19T1 Load Transient Response



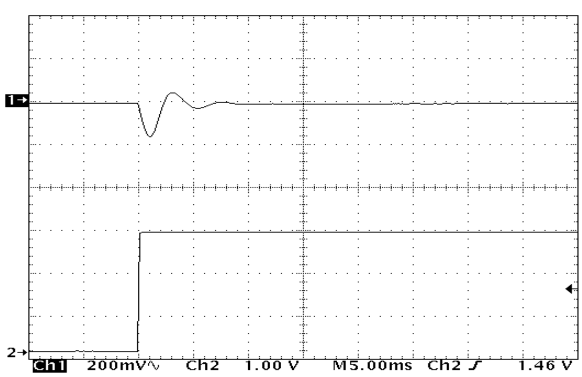
V_{IN} = 2.0 V, L = 4.7 μH, C_{OUT} = 220 μF
1. V_{OUT}, 3.0 V (AC coupled), 200 mV/div
2. I_O, 1.0 mA to 100 mA

Figure 59. NCP1450ASN30T1 Load Transient Response



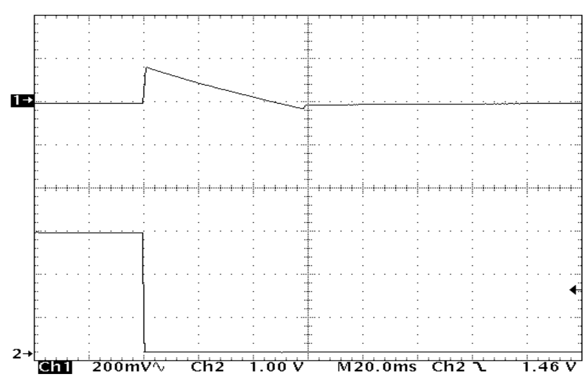
V_{IN} = 2.0 V, L = 4.7 μH, C_{OUT} = 220 μF
1. V_{OUT}, 3.0 V (AC coupled), 200 mV/div
2. I_O, 100 mA to 1.0 mA

Figure 60. NCP1450ASN30T1 Load Transient Response



V_{IN} = 3.0 V, L = 4.7 μH, C_{OUT} = 220 μF
1. V_{OUT}, 5.0 V (AC coupled), 200 mV/div
2. I_O, 1.0 mA to 100 mA

Figure 61. NCP1450ASN50T1 Load Transient Response



V_{IN} = 3.0 V, L = 4.7 μH, C_{OUT} = 220 μF
1. V_{OUT}, 5.0 V (AC coupled), 200 mV/div
2. I_O, 100 mA to 1.0 mA

Figure 62. NCP1450ASN50T1 Load Transient Response

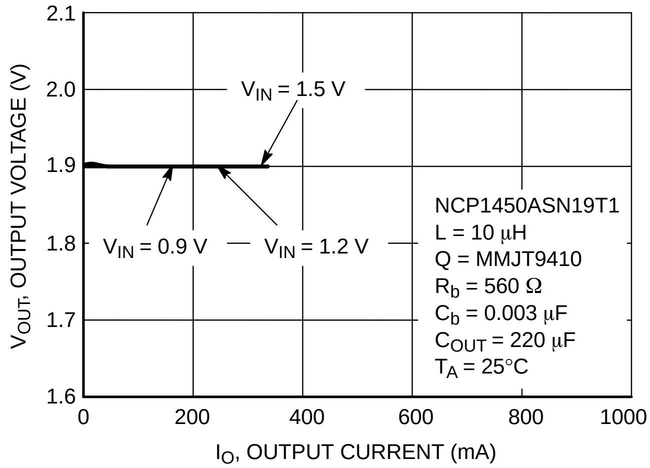


Figure 63. NCP1450ASN19T1 Output Voltage vs. Output Current (Ext. BJT)

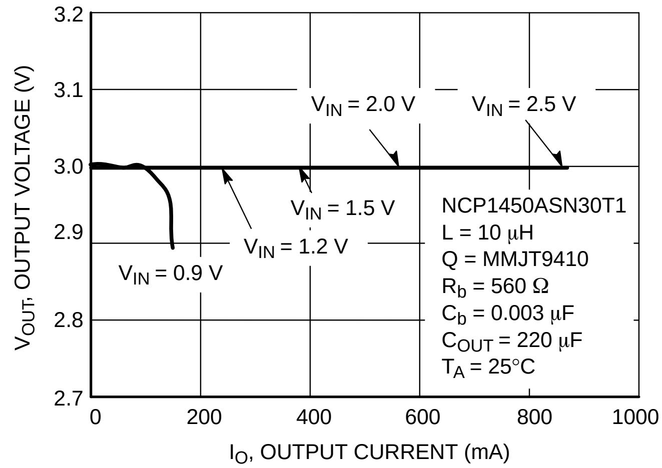


Figure 64. NCP1450ASN30T1 Output Voltage vs. Output Current (Ext. BJT)

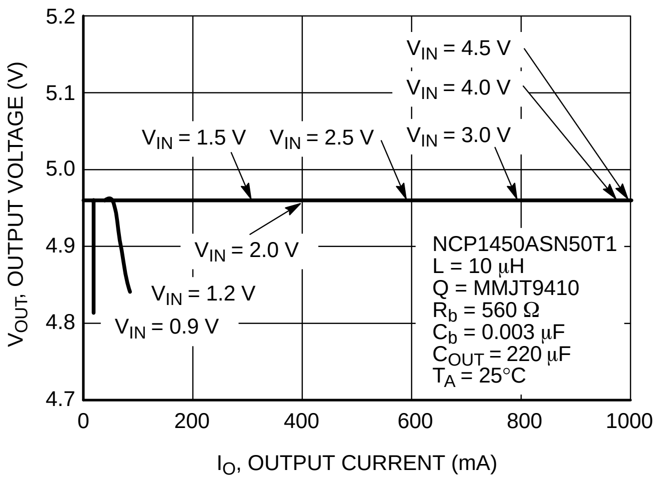


Figure 65. NCP1450ASN50T1 Output Voltage vs. Output Current (Ext. BJT)

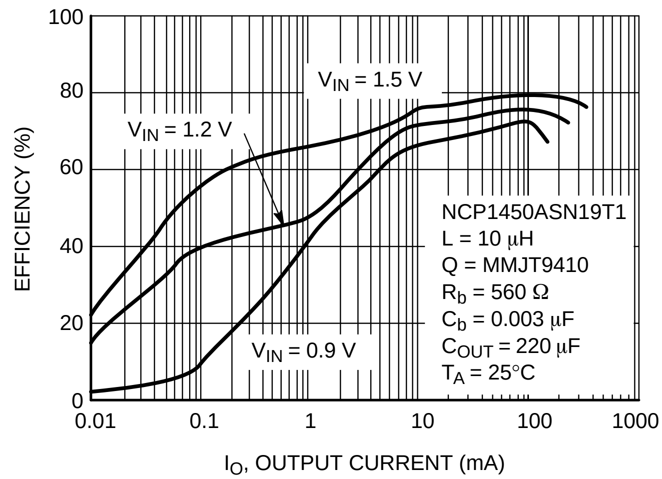


Figure 66. NCP1450ASN19T1 Efficiency vs. Output Current (Ext. BJT)

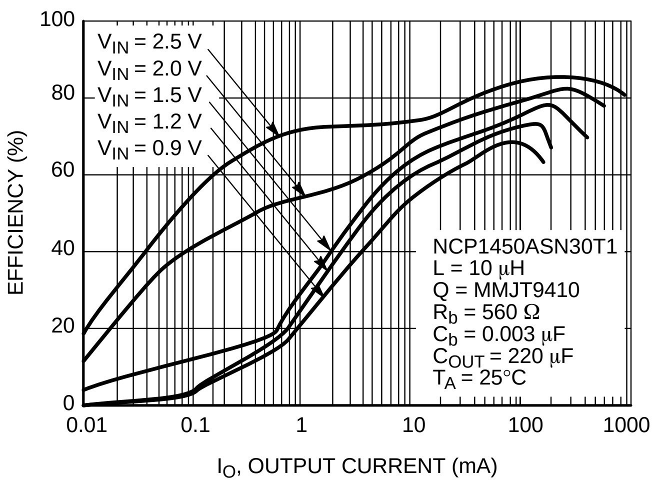


Figure 67. NCP1450ASN30T1 Efficiency vs. Output Current (Ext. BJT)

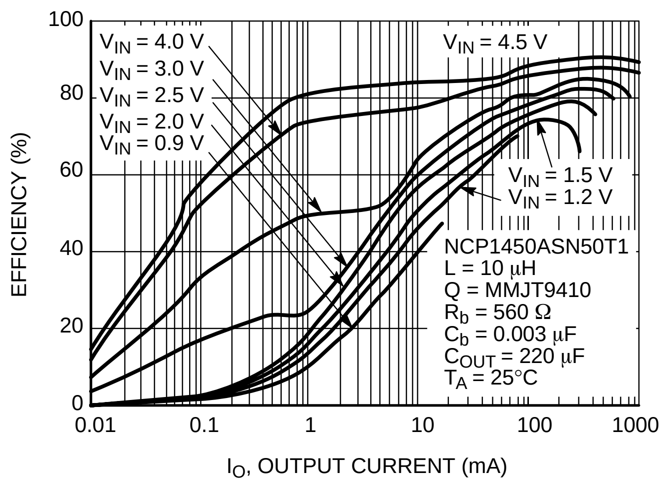


Figure 68. NCP1450ASN50T1 Efficiency vs. Output Current (Ext. BJT)

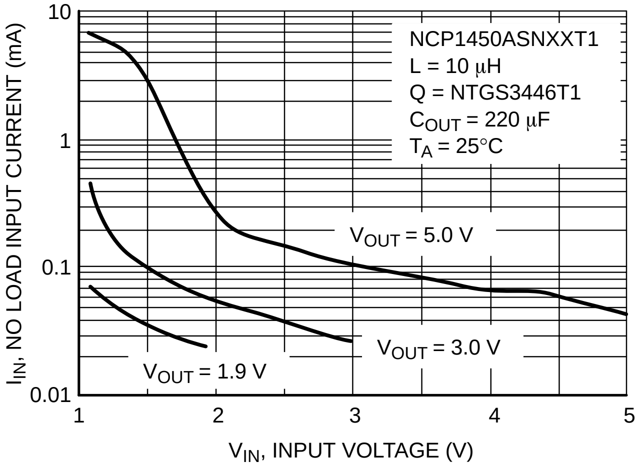


Figure 69. NCP1450ASNXXT1 No Load Input Current vs. Input Voltage (Using MOSFET)

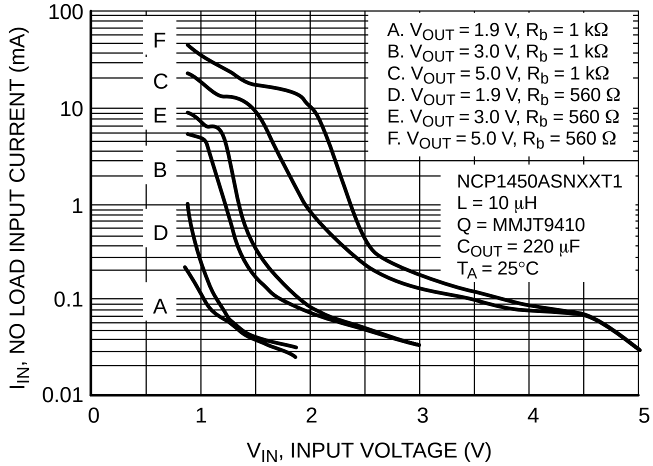


Figure 70. NCP1450ASNXXT1 No Load Input Current vs. Input Voltage (Using BJT)

Components Supplier

Parts	Supplier	Part Number	Description	Phone
Inductor: L1, L2	Sumida Electric Co. Ltd.	CD54−100MC	Inductor 10 μH/1.44 A	(852) 2880−6688
Schottky Diode: D1, D2	ON Semiconductor	MBRM110L	Schottky Power Rectifier	(852) 2689−0088
MOSFET: Q1	ON Semiconductor	NTGS3446T1	Power MOSFET N−Channel	(852) 2689−0088
BJT: Q2	ON Semiconductor	MMJT9410	Bipolar Power Transistor	(852) 2689−0088
Output Capacitor: C1, C3	KEMET Electronics Corp.	T494D227K006AS	Low ESR Tantalum Capacitor 220 μF/6.0 V	(852) 2305−1168
Input Capacitor: C2, C4	KEMET Electronics Corp.	T491C106K016AS	Low Profile Tantalum Capacitor 10 μF/16 V	(852) 2305−1168

DETAILED OPERATING DESCRIPTION

Operation

The NCP1450A series are monolithic power switching controllers optimized for battery powered portable products where large output current is required.

The NCP1450A series are low noise fixed frequency voltage−mode PWM DC−DC controllers, and consist of startup circuit, feedback resistor divider, reference voltage, oscillator, loop compensation network, PWM control circuit, and low ON resistance driver. Due to the on−chip feedback resistor and loop compensation network, the system designer can get the regulated output voltage from 1.8 V to 5.0 V with 0.1 V stepwise with a small number of external components. The quiescent current is typically 93 μA (V_{OUT} = 2.7 V, f_{OSC} = 180 kHz), and can be further reduced to about 1.5 μA when the chip is disabled (V_{CE} < 0.3 V).

The NCP1450A operation can be best understood by referring to the block diagram in Figure 2. The error amplifier monitors the output voltage via the feedback resistor divider by comparing the feedback voltage with the reference voltage. When the feedback voltage is lower than the reference voltage, the error amplifier output will decrease. The error amplifier output is then compared with the oscillator ramp voltage at the PWM controller. When the ramp voltage is higher than the error amplifier output, the high−side driver is turned on and the low−side driver is turned off which will then switch on the external transistor; and vice versa. As the error amplifier output decreases, the high−side driver turn−on time increases and duty cycle increases. When the feedback voltage is higher than the reference voltage, the error amplifier output increases and the duty cycle decreases. When the external power switch is on, the current ramps up in the inductor, storing energy in the magnetic field. When the external power switch is off, the energy stored in the magnetic field is transferred to the output filter capacitor and the load. The output filter capacitor stores the charge while the inductor current is higher than the output current, then sustains the output voltage until the next switching cycle.

As the load current is decreased, the switch transistor turns on for a shorter duty cycle. Under the light load condition, the controller will skip switching cycles to reduce power consumption, so that high efficiency is maintained at light loads.

Soft Start

There is a soft start circuit in NCP1450A. When power is applied to the device, the soft start circuit first pumps up the output voltage to approximately 1.5 V at a fixed duty cycle. This is the voltage level at which the controller can operate normally. In addition to that, the startup capability with heavy loads is also improved.

Oscillator

The oscillator frequency is internally set to 180 kHz at an accuracy of ±20% and with low temperature coefficient of 0.11%/°C.

Regulated Converter Voltage (V_{OUT})

The V_{OUT} is set by an integrated feedback resistor network. This is trimmed to a selected voltage from 1.8 V to 5.0 V range in 100 mV steps with an accuracy of ±2.5%.

Compensation

The device is designed to operate in continuous conduction mode. An internal compensation circuit was designed to guarantee stability over the full input/output voltage and full output load range.

Enable/Disable Operation

The NCP1450A series offer IC shutdown mode by chip enable pin (CE pin) to reduce current consumption. When voltage at pin CE is equal or greater than 0.9 V, the chip will be enabled, which means the controller is in normal operation. When voltage at pin CE is less than 0.3 V, the chip is disabled, which means IC is shutdown.
Important: DO NOT apply a voltage between 0.3 V to 0.9 V to pin CE as this is the CE pin’s hysteresis voltage range. Clearly defined output states can only be obtained by applying voltage out of this range.

APPLICATION CIRCUIT INFORMATION

Step−up Converter Design Equations

The NCP1450A PWM step−up DC−DC controller is designed to operate in continuous conduction mode and can be defined by the following equations. External components values can be calculated from these equations, however, the optimized value should obtained through experimental results.

Calculation	Equation
D	$\le \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - V_S}$
I_L	$\frac{I_O}{(1 - D)}$
L	$\frac{(V_{OUT} + V_D - V_{IN})(1 - D)^2}{f \times I_O \times DIR}$
I_{PK}	$I_L(1 + \frac{DIR}{2})$
ΔQ	$\frac{(I_L - I_O)(1 - D)}{f}$
V_{PP}	$\approx \frac{\Delta Q}{C_{OUT}} + (I_L - I_O)\ ESR$

NOTES:
- D − On−time duty cycle
- I_L − Average inductor current
- I_{PK} − Peak inductor current
- DIR − Delta inductor current to average inductor current ratio
- I_O − Desired dc output current
- V_{IN} − Nominal operating dc input voltage
- V_{OUT} − Desired dc output voltage
- V_D − Diode forward voltage
- V_S − Saturation voltage of the external transistor switch
- ΔQ − Charge stores in the C_{OUT} during charging up
- ESR − Equivalent series resistance of the output capacitor

Design Example

It is supposed that a step−up DC−DC controller with 3.3 V output delivering a maximum 1000 mA output current with 100 mV output ripple voltage powering from a 2.4 V input is to be designed.

Design parameters:

V_{IN} = 2.4 V
V_{OUT} = 3.3 V
I_O = 1.0 A
V_{pp} = 100 mV
f = 180 kHZ
DIR = 0.2 (typical for small output ripple voltage)

Assume the diode forward voltage and the transistor saturation voltage are both 0.3 V. Determine the maximum steady state duty cycle at V_{IN} = 2.4 V:

$$D = \frac{3.3V + 0.3V - 2.4V}{3.3V + 0.3V - 0.3V} = 0.364$$

Calculate the maximum inductance value which can generate the desired current output and the preferred delta inductor current to average inductor current ratio:

$$L \le \frac{(3.3V + 0.3V - 2.4V)(1 - 0.364)^2}{180000\,Hz \times 1A \times 0.2} = 13.5\mu H$$

Determine the average inductor current and peak inductor current:

$$I_L = \frac{1}{1 - 0.364} = 1.57A$$

$$I_{PK} = 1.57A\ (1 + \frac{0.2}{2}) = 1.73A$$

Therefore, a 12 μH inductor with saturation current larger than 1.73 A can be selected as the initial trial.

Calculate the delta charge stored in the output capacitor during the charging up period in each switching cycle:

$$\Delta Q = \frac{(1.57A - 1A)(1 - 0.364)}{18000Hz} = 2.01\mu C$$

Determine the output capacitance value for the desired output ripple voltage:

Assume the ESR of the output capacitor is 0.15 Ω,

$$C_{OUT} > \frac{2.01\mu C}{100mV - (1.57A - 1A) \times 0.15\Omega} = 138.6\mu F$$

Therefore, a Tantalum capacitor with value of 150 μF to 220 μF and ESR of 0.15 Ω can be used as the output capacitor. However, according to experimental result, 220 μF output capacitor gives better overall operational stability and smaller ripple voltage.

External Component Selection

Inductor Selection

The NCP1450A is designed to work well with a 6.8 to 12 μH inductors in most applications 10 μH is a sufficiently low value to allow the use of a small surface mount coil, but large enough to maintain low ripple. Lower inductance values supply higher output current, but also increase the ripple and reduce efficiency.

Higher inductor values reduce ripple and improve efficiency, but also limit output current.

The inductor should have small DCR, usually less than 1 Ω, to minimize loss. It is necessary to choose an inductor with a saturation current greater than the peak current which the inductor will encounter in the application.

Diode

The diode is the largest source of loss in DC−DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, V_D , and the reverse recovery time, trr. The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P−N junction. A Schottky diode with the following characteristics is recommended:

Small forward voltage, $V_F < 0.3$ V

Small reverse leakage current

Fast reverse recovery time/switching speed

Rated current larger than peak inductor current, $I_{rated} > I_{PK}$

Reverse voltage larger than output voltage, $V_{reverse} > V_{OUT}$

Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small Equivalent Series Resistance (ESR) Tantalum or ceramic capacitor with a value of 10 μF should be suitable.

Output Capacitor

The output capacitor is used for sustaining the output voltage when the external MOSFET or bipolar transistor is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a 100 μF to 220 μF low ESR (0.10 Ω to 0.30 Ω) Tantalum capacitor should be appropriate.

External Switch Transistor

An enhancement N−channel MOSFET or a bipolar NPN transistor can be used as the external switch transistor.

For enhancement N−channel MOSFET, since enhancement MOSFET is a voltage driven device, it is a more efficient switch than a BJT transistor. However, the MOSFET requires a higher voltage to turn on as compared with BJT transistors. An enhancement N−channel MOSFET can be selected by the following guidelines:

1. Low ON−resistance, $R_{DS(on)}$, typically < 0.1 Ω.
2. Low gate threshold voltage, $V_{GS(th)}$, must be < V_{OUT}, typically < 1.5 V, it is especially important for the low V_{OUT} device, like V_{OUT} = 1.9 V.
3. Rated continuous drain current, I_D, should be larger than the peak inductor current, i.e. $I_D > I_{PK}$.
4. Gate capacitance should be 1200 pF or less.

For bipolar NPN transistor, medium power transistor with continuous collector current typically 1 A to 5 A and $V_{CE(sat)}$ < 0.2 V should be employed. The driving capability is determined by the DC current gain, H_{FE}, of the transistor and the base resistor, Rb; and the controller’s EXT pin must be able to supply the necessary driving current.

Rb can be calculated by the following equation:

$$Rb = \frac{V_{OUT} - 0.7}{Ib} - \frac{0.4}{|I_{EXTH}|}$$

$$Ib = \frac{I_{PK}}{H_{FE}}$$

Since the pulse current flows through the transistor, the exact Rb value should be finely tuned by the experiment. Generally, a small Rb value can increase the output current capability, but the efficiency will decrease due to more energy is used to drive the transistor.

Moreover, a speed−up capacitor, Cb, should be connected in parallel with Rb to reduce switching loss and improve efficiency. Cb can be calculated by the equation below:

$$Cb \le \frac{1}{2\pi \times Rb \times f_{OSC} \times 0.7}$$

It is due to the variation in the characteristics of the transistor used. The calculated value should be used as the initial test value and the optimized value should be obtained by the experiment.

External Component Reference Data

Device	V_{OUT}	Inductor Model	Inductor Value	External Transistor	Diode	Output Capacitor
NCP1450ASN19T1	1.9 V	CD54	12 μH	NTGS3446T1	MBRM110L	220 μF
NCP1450ASN30T1	3.0 V	CD54	10 μH	NTGS3446T1	MBRM110L	220 μF
NCP1450ASN50T1	5.0 V	CD54	10 μH	NTGS3446T1	MBRM110L	220 μF
NCP1450ASN19T1	1.9 V	CD54	12 μH	MMJT9410	MBRM110L	220 μF
NCP1450ASN30T1	3.0 V	CD54	10 μH	MMJT9410	MBRM110L	220 μF
NCP1450ASN50T1	5.0 V	CD54	10 μH	MMJT9410	MBRM110L	220 μF

An evaluation board of NCP1450A has been made in the small size of 89 mm x 51 mm. The artwork and the silk screen of the surface−mount evaluation board PCB are shown in Figures 71 and 72. Please contact your ON Semiconductor representative for availability. The evaluation board schematic diagrams are shown in Figures 73 and 74.

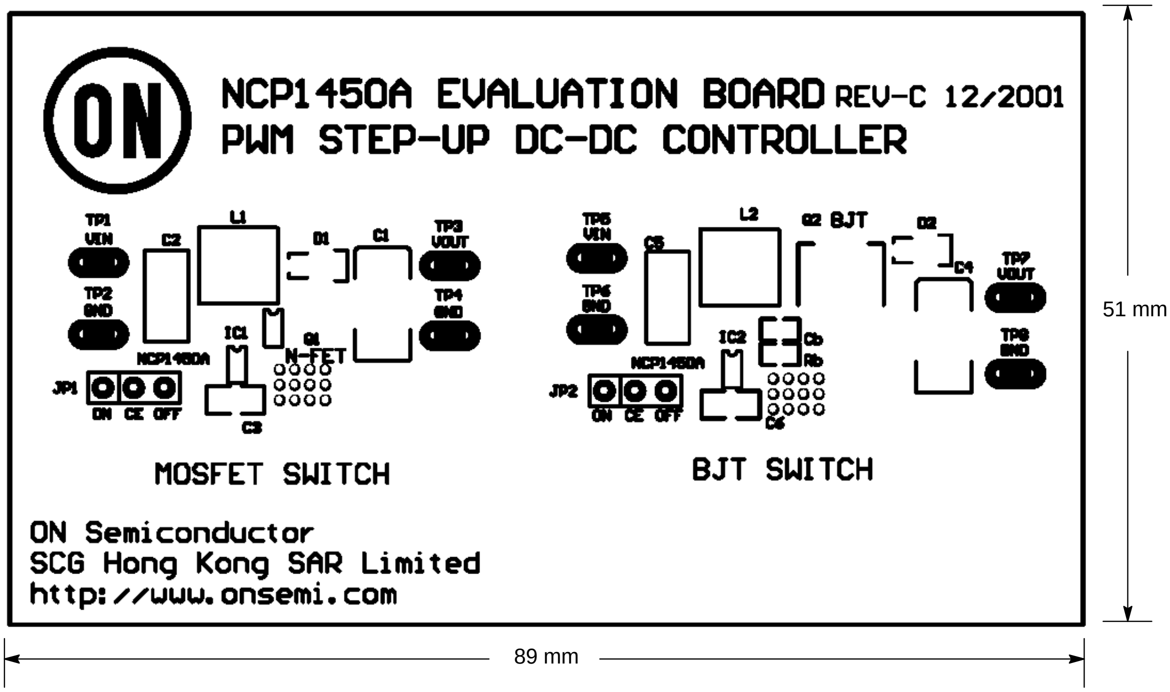


Figure 71. NCP1450A PWM Step−up DC−DC Controller Evaluation Board Silkscreen

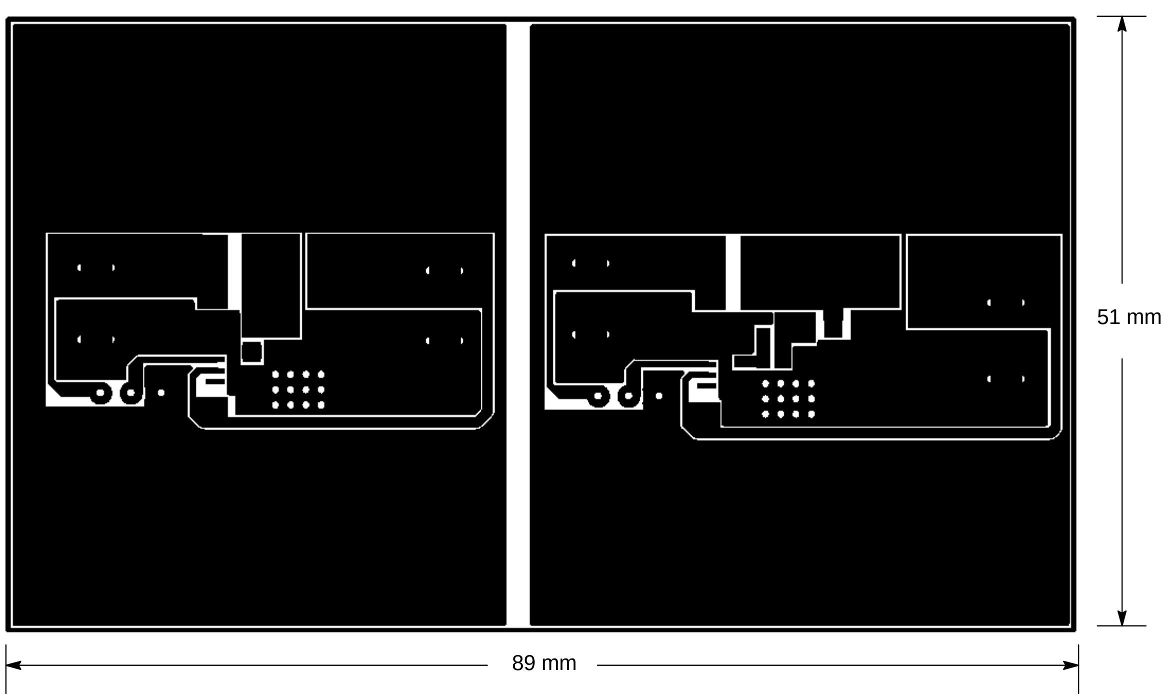


Figure 72. NCP1450A PWM Step−up DC−DC Controller Evaluation Board Artwork (Component Side)

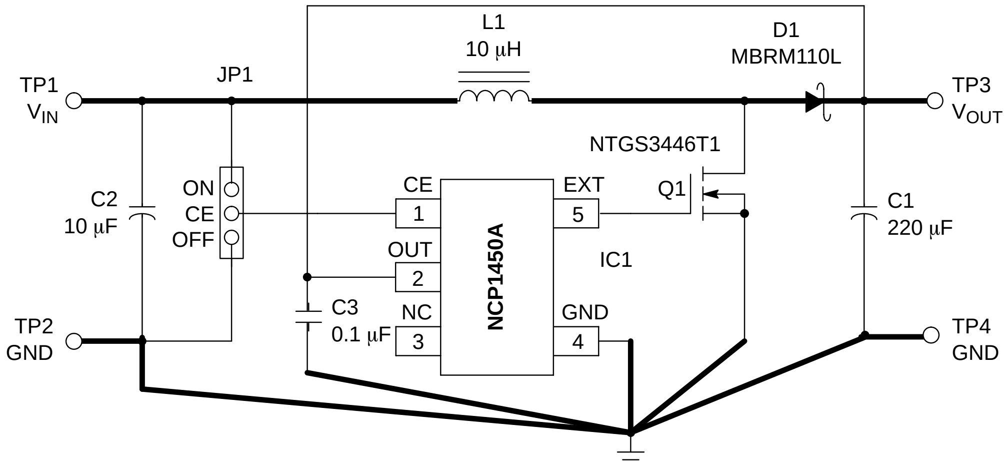


Figure 73. NCP1450A Evaluation Board Schematic Diagram 1 (Step−up DC−DC Converter Using External MOSFET Switch)

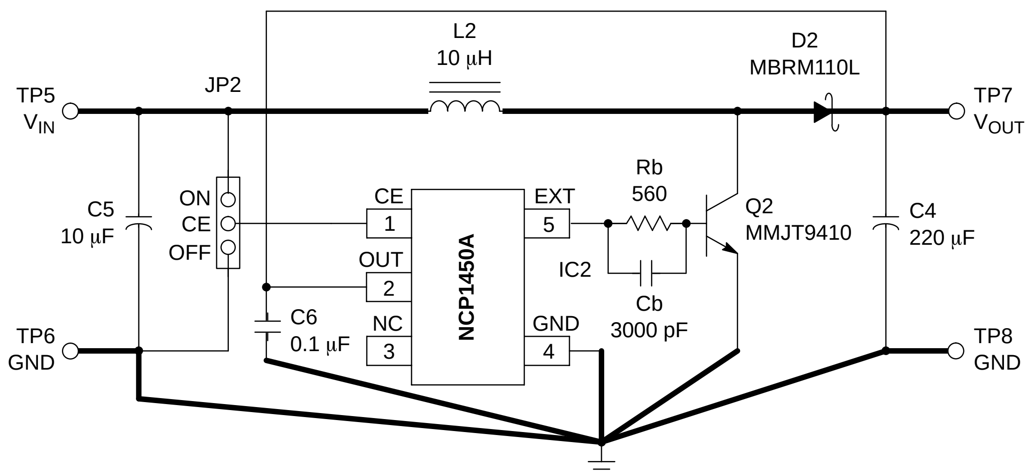


Figure 74. NCP1450A Evaluation Board Schematic Diagram 2 (Step−up DC−DC Converter Using External Bipolar Transistor Switch)

PCB Layout Hints

Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise. In Figure 73, e.g.: C2 GND, C1 GND, and IC1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g.: short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to anode pin of D1
3. Trace from cathode pin of D1 to TP3

Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.

Switching Noise Decoupling Capacitor

A 0.1 μF ceramic capacitor should be placed close to the OUT pin and GND pin of the NCP1450A to filter the switching spikes in the output voltage monitored by the OUT pin.

PACKAGE DIMENSIONS

TSOP−5
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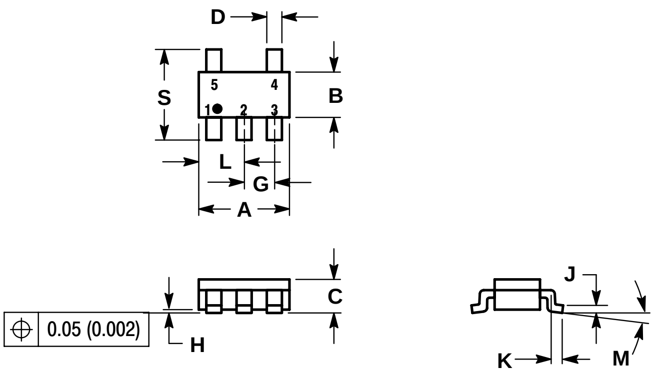
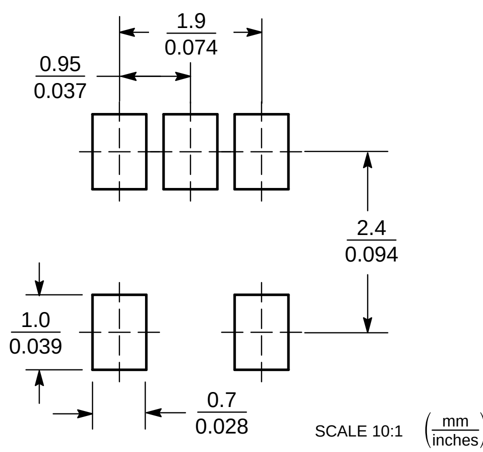
CASE 483−02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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